REMARKS

The original filing of the present application included Claims 1-9. No additions of claims have been made in the prosecution of the present application. Claims 1-7 are currently pending in the present application with claims 1 and 7 being amended by this response. Claims 8 and 9 have been cancelled by a previous amendment. Claims 1-7 stand rejected in the Office Action dated September 9, 2003 and this amendment addresses the rejections made in this Office Action.

Rejection of Claims 1-6 under 35 U.S.C. § 102(b)

Claims 1-6 stand rejected under 35 U.S.C. §102(b) as being anticipated by Shinya, U.S. Patent No. 5,170,158.

The present claimed invention is an arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device. The arrangement includes a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal. The plurality of semiconductor switches are separated into groups of semiconductor switches and the groups of semiconductor switches are separated into subgroups of semiconductor switches. A control bus has a plurality of conductors. Each conductor is coupled to the first terminal of each of the plurality of semiconductor switches in a respective subgroup for communicating corresponding signals. A plurality of local buses that are separated from one another are provided for communicating corresponding signals. Each of the plurality of local buses are associated with a respective group of semiconductor switches and have a plurality of conductors. Each of the plurality of conductors have a first bus section extending in a manner to cross the plurality of conductors of the control bus once and a second bus section connected to an end of the first bus section. The second bus section is coupled in a local, clustering bus arrangement to the second terminal of a respective semiconductor switch within each subgroup of the respective group of semiconductor switches. The associated switches have the third terminals

thereof coupled to the consecutively disposed column conductors of the array of the display device.

The configuration of the buses in the present claimed invention inherently decreases the number of times the local buses cross over the control bus. The disadvantages associated with crossing of the control bus are described with reference to Figure 2 of the inventive disclosure, specifically on page 6 lines 10-14, addressing the fact that

> "the number of capacitive crossovers increases geometrically with the number of data-word conductors DW(i) according to the equation: number of crossovers = number of brightness information carrying conductors DB(j) x 1/2 x (number of data-word conductors DW(i))."

The present claimed invention reduces the number of times conductors DWC(i) cross the bus of conductors DW(i) in order to reduce dynamic power dissipation and improve yield by coupling the plurality of local buses to the second terminal of the plurality of switches in a clustering bus arrangement. The inventive application discusses its achievement of the stated objective with reference to Figure 3 stating on page 6, lines 17-29, summarizing on lines 24-29:

> "In this example, the number of crossovers of brightness information carrying conductors DB (j)-to-data-word conductors DW (i) have been reduced by a factor of about 4:1. This, advantageously, reduces dynamic power dissipation, improves yield and reduces the crosstalk among the brightness information carrying-conductors."

On page 7, lines 18-20, the interconnections of the prior art diagram shown in Figure 2 and the inventive diagram on Figure 3 are compared as 28,800 crossovers are present in the prior art and only 7,450 total crossovers are present in the present claimed invention.

Furthermore, the claimed plurality of local buses which are separated from one another in the local clustering bus arrangement reduces the capacitance formed between the local buses. As is claimed in claim 1 and can be seen in Figure 3, each local bus is associated with a respective group of switches whereby a given one of said plurality of local buses having a first bus section coupled to said second terminal of respective ones of said plurality of semiconductor switches.

Shinya discloses a display device having a driver circuit for driving data lines in a matrix display panel according to input digital signals. The driver circuit includes a number of digital-to-analog (D/A) converters, which number is less than the number of pixels contained in one horizontal scanning line. The D/A converters are repeatedly used to sequentially convert portions of the input digital image signal corresponding to one horizontal scanning line. The analog signals obtained by each D/A conversion are retained by a sample-and-hold circuit. When storage for one horizontal scanning line is completed, the signals are simultaneously delivered to the data lines.

Shinya neither discloses nor suggests "a plurality of semiconductor switches... being separated into groups of semiconductor switches and said groups of semiconductor switches being separated into subgroups of semiconductor switches" as in the present claimed invention. Shinya discloses a plurality of switches. However, the switches are not separated into groups and subgroups as in the present claimed invention. The separation of the switches into groups and subgroups within each group allows the present claimed invention to accomplish the objective of minimizing capacitive shorting failures, cross talk among the brightness information carrying conductors and dynamic power dissipation. Such is not accomplished by the device of Shinya. Shinya also neither discloses nor suggests "a plurality of local buses that are separated from one another... each of said plurality of local buses being associated with a respective group of semiconductor switches and having a plurality of conductors having a first bus section" as in the present claimed invention. Shinya, as illustrated in Figure 2 connects a DAC 15 to a number of sample and hold circuits. Each DAC 15 inputs a digital image signal corresponding to a set of twenty pixels into one sample and hold circuit 16, placing a digital image signal corresponding to a next set of twenty

pixels into another sample and hold circuit 16. Shinya only discloses a plurality of individual conductors all crossing over one another. Such is shown and described in the figures whereby the control lines cross each conductor numerous times. As discussed above, this configuration is contrary to the purpose of the present claimed invention. In this embodiment, each individual conductor crosses a first section of the control bus and then each conductor of the control bus crosses each conductor of the local bus a plurality of times. Thus, a capacitive coupling is incurred at each cross over as discussed in the present specification with respect to the prior art figure 2. In the present claimed invention a plurality of local buses, each local bus including a plurality of conductors, are separated from one another and have a plurality of conductors coupled in a local, clustering bus arrangement. This configuration minimizes the number of crossovers in order to reduces dynamic power dissipation, improve yield and reduce crosstalk among the brightness information carrying-conductors. Shinya is concerned with reducing the number of DAC's and thereby reducing the size of the display device as opposed to the present claimed invention which is concerned with improving the yield and reducing crosstalk among the conductors.

Shinya also neither discloses nor suggests "a control bus having a plurality of conductors, each conductor being coupled to said first terminal of each of said plurality of semiconductor switches in a respective subgroup of each group of semiconductor switches for communicating corresponding signals" as in the present claimed invention. Additionally, Shinya includes a control bus coupled to a selective group of sample and hold circuits, i.e. the first 20 sample and hold circuits. This is unlike the present claimed invention in which the control bus is connected to a control terminal of each switch in a subgroup of switches of each group of switches. Furthermore, Shinya neither discloses nor suggests the local buses "having a first bus section extending in a manner to cross said plurality of conductors of said control bus once and a second bus section connected to an end of said first bus section and coupled in a local, clustering bus arrangement to the second terminal of a respective semiconductor switch within each subgroup of the respective group of semiconductor switches" as in the present claimed invention. None of the data buses of Shinya have a first section which crosses each of the conductors of a control bus as in the present claimed invention. The data

buses of Shinya also do not include a second section coupled to an end of the first section as in the present claimed invention.

Accordingly, it is respectfully submitted that the present claimed invention is not anticipated by Shinya and that the rejection of Claim 1 under 35 U.S.C. § 102(b) is satisfied. Additionally, because Claims 2-6 depend from the independent Claim 1, dependent claims 2-6 also satisfy this rejection for the same reason as Claim 1. In view of the above remarks it is respectfully submitted this rejection of claims 1-6 be withdrawn.

Rejection of Claim 7-9 under 35 U.S.C. § 102(b)

Claims 7-9 stand rejected under 35 U.S.C. §102(b) as being anticipated by Inoue et al., U.S. Patent No. 5,113,181.

The present invention as claimed in claim 7 recites a signal demultiplexer for a display panel. The signal demultiplexer includes a plurality of switch groups. Each switch group includes a plurality of subgroups. Each subgroup has ordinally numbered switches 1 thru n arranged sequentially. Each switch has respective input, output and control terminals with the control terminals of all switches in each subgroup being connected to a common control terminal, and having respective output terminals coupled to successive data lines on the display panel. A plurality of groups of data buses are each associated with a respective switch group. The groups of data buses have ordinally numbered conductors 1 thru n. The ordinally numbered conductors of respective groups of data buses are coupled to input terminals of a corresponding. A control bus includes a plurality of conductors and is arranged to cross the plurality of groups of data buses. Connections are provided between ones of the plurality of conductors of said control bus and a common control terminal of a respective subgroup within each of said plurality of switch groups.

Inoue et al. describes a display apparatus comprising a plurality of pixels arranged in pluralities of rows and columns. This apparatus includes an N X M active

matrix liquid crystal display unit having N X M pixels, each pixel being provided with a switching element. Image signal lines supply latched image signals to the switching elements and switching lines switch the switching elements. The image signal lines are divided into n blocks each having m lines which are commonly connected to one signal line through a corresponding switching element. The n lines are selectively supplied an image signal through the switching element by the image signal line, the image signal being stored in a capacitor.

Inoue et al. neither disclose nor suggest "a plurality of switch groups, each switch group including a plurality of subgroups, each subgroup having ordinally numbered switches 1 thru n arranged sequentially, and each switch having respective input, output and control terminals with the control terminals of all switches in each subgroup being connected to a common control terminal" as in the present claimed invention. Inoue et al. includes a plurality of switch groups. However, the switches within each group are not divided into subgroups with the control terminal of each switch within a subgroup connected to a common control terminal as in the present claimed invention. Inoue et al. also neither disclose nor suggest "a plurality of groups of data buses, each group of data buses being associated with a respective switch group and having ordinally numbered conductors 1 thru n, the ordinally numbered conductors of respective groups of data buses being coupled to input terminals of a corresponding ordinally numbered switch of each subgroup within the respective switch" as in the present claimed invention. Inoue et al. disclose a plurality of signal lines, each signal line being coupled to an input terminal of one switch in each switch group. Furthermore, Inoue et al. neither discloses nor suggests the local buses "having a first bus section extending in a manner to cross said plurality of conductors of said control bus once and a second bus section connected to an end of said first bus section and coupled in a local, clustering bus arrangement to the second terminal of a respective semiconductor switch within each subgroup of the respective group of semiconductor switches" as in the present claimed invention. None of the data buses of Inoue et al. have a first section which crosses each of the conductors of a control bus as in the present claimed invention. In the arrangement of Inoue et al. none of the data buses will cross the plurality of control

buses. The data buses of Shinya also do not include a second section coupled to an end of the first section as in the present claimed invention.

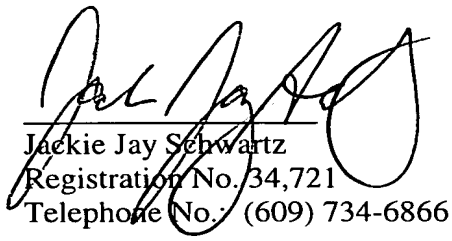
As explained above the present claimed invention reduces dynamic power dissipation and improve yield by reducing the number of times conductors DWC(i) cross the bus of conductors DW(i). The claimed configuration of the data and control buses of the present claimed invention is able to accomplish these objectives. Inoue et al. is concerned with reducing the number of signal lines to reduce cost, simplify production and minimize delay of polarity. Inoue et al. is not concerned with reducing dynamic power dissipation and improve yield by reducing the number of times the conductors DWC (i) cross the bus of conductors DW (i) as in the present claimed invention. In fact, the arrangement of Inoue et al., which uses a plurality of conductive lines and a plurality of switching signal lines, increases the number of crossovers and thereby increases the capacitive coupling between the conductors. As reducing dynamic power dissipation and improve yield by reducing the number of times the local buses cross the control bus as in the present claimed invention is not a concern of Inoue et al. Inoue et al. neither discloses nor suggests such an embodiment in which a plurality of groups of data buses are crossed by the control bus as in the present claimed invention. Inoue et al. neither discloses use of a data bus or control bus but only discloses a plurality of individual conductive lines.

Accordingly, it is respectfully submitted that the present invention as claimed in Claim 7 is not anticipated by Inoue et al. Claims 8 and 9 were cancelled by a previous response and thus it is respectfully submitted that the rejection of these claims is moot and should be withdrawn. It is thus further respectfully submitted that this rejection under 35 U.S.C. § 102(b) is satisfied and should be withdrawn.

In view of all of the foregoing, it is submitted that the amended application is now in condition for allowance, and such action is respectfully requested.

No additional fee is believed due with this amendment. However, if an additional fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
Roger Green Stewart



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